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Efficient Designs of Ripple Carry Adders Using QCA

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Abstract: A quantum-dot cellular automaton (QCA) is a novel nanotechnology that promotes high-performance computation with low heat dissipation, where a quantum dot has a geometric symmetry. The half adder, full adder and Ripple Carry Adders are the basic components of every arithmetic circuit. In this paper, the benefits of QCA will be used to propose the basic arithmetic components. A QCA design for XOR gate will be proposed. The proposed QCA for the XOR gate will be used to implement half adder and full adder circuits. The proposed QCA for full adder circuit will be used to design Ripple Carry Adders (RCA) with different sizes such as 4-bit, 8-bit, and 16-bit RCA. The clock cycle delay and energy dissipation for the proposed designs are calculated. Comparing the proposed QCA designs with related designs in literature shows that the proposed QCA designs are more efficient in terms of cell count, construction area, number of majority gates, wire crossing, and/or clock cycle latency.

Keywords: Quantum-dot Cellular Automata; Half Adder Circuit; Full Adder Circuit; Ripple Carry Adders Circuits; XOR Gate.

1 Introduction

Building computational devices based on dense integrated circuits technology is reaching its limit where Moore's law is no longer applied [1]. There is a need for alternative technologies to be able to build more powerful computational devices. A quantum dot cellular automata (QCA) is an emerging viable technology that can be used to build the next-generation computational devices [2]. QCA is a nanotechnology that combines high computational performance with low heat

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dissipation. QCA is a technology for developing nanoelectronics and nano-level computational devices [3]. It was shown that symmetric functions can be implemented using QCA [4], and the symmetric group of the geometry for quantum dot has been investigated [5]. Recently, designing computational circuits such as half adder, full adder, and Ripple Carry Adders using QCA technology is gaining attention. QCA can be used to improve nano electronic devices by increasing the speed, decreasing the size of the components, and minimizing power dissipation. QCA depends on binary information that is encoded inside the quantum dot cells within an electron charge arrangement. Computational power between the QCA cells is generated due to the coulombic interaction between the cells. Due to the arrangement of electron positions, the interaction of cell-to-cell physics provides the local interconnections between cells [6, 7]. Tougaw and Lent [8, 9] introduced the basic principle of QCA as arrays of quantum-dot cells in 1993. In QCA, a cell is the basic unit that represents the logic state. A cell is a nanoscale device that can store information by arranging two electrons in a specific pattern [10]. Errors may occur due to misalignment and fabrication errors, so the cells should be adjusted at nanoscales to give the proper function. The adjustment of these cells will lead to circuit correction [11].

The main aim of this paper is to propose QCA designs for XOR gate, half adder circuit, full adder circuit, where different sizes of Ripple Carry Adders (RCA) circuits such as 4-bit, 8-bit, and 16-bit RCA will be proposed. The XOR gate has been used to design half adder and full adder circuits. A QCA design for full adder circuit has been used to implement a QCA design for RCA with different sizes. The proposed designs are using single layer and coplanar designs. The energy dissipation of the proposed designs are calculated using QCADesigner-E simulator. The proposed designs will be shown to be better in terms of cell counts, area used in the construction, number of majority gate, wire crossover, and/or clock cycle delay than the proposed designs in literature.

The paper is organized as follows: the related work is discussed in Section 2. Section 3 reviews the QCA fundamentals and the clocking basics. Section 4 proposes the QCA designs for arithmetic circuits. Section 5 discusses the energy dissipation for the proposed circuits, and the paper is finally concluded in Section 6.

2 Related Works

In [12-17], many QCA designs for XOR gate have been presented. In 2015, a QCA design has been proposed with 32 cells and 1 clock delay [12]. In 2019, a QCA design consists of 17 cells and 2 clock cycle delay [15], which is better than the design in [12] in terms of cell count. In 2021, another QCA design for XOR gate has been proposed in [16] with 9 cells and 0.25 clock cycle delay. In 2022, a proposed QCA design with 26 cells and 3 clock cycle delay [17]. Comparing with the design in [16], the design in [17] is not efficient in terms of cell count, area used in the construction, and clock cycle delay.

Many designs for half adder circuit have been proposed in [18-23]. In 2013, a proposed QCA design in [18] consists of 77 cells with 4 clock delay. In 2018, a proposed design in [21] contains 27 cells with 0.5 clock delay. In 2019, a QCA design for half adder circuit has been proposed with 48 cells and 0.5 clock cycle delay [22]. In 2022, another QCA half adder circuit design in [23] with 26 cells and 0.5 clock cycle delay, this design is more efficient in terms of cell count and clock cycle delay with respect to the other previous designs.

Many designs for QCA full adder circuit have been proposed in [15, 17, 18, 24-32]. In 2013, a proposed QCA design in [18] for multilayer full adder circuit with large

number of cell count is proposed where it contains 122 cells and 4 clock delay. In 2019, a QCA design has been proposed using 49 cells and with 4 clock cycle delay [15]. In 2021, a QCA design has been proposed in [32] with 30 cells and 0.5 clock cycle delay. In 2022, a QCA design for multilayer full adder circuit with 86 cells and 3 clock delay has been proposed [17]. The design in [17] is not efficient in terms of cell count compared with design in [32, 15] and better than the design in [18] in terms of cell count and clock cycle delay.

Many QCA designs have been proposed for 4-bit RCA in [28-31, 33]. In 2016, a proposed QCA multilayer design in [29] for 4-bit RCA with 237 cells and 6 clock cycle delay. In 2018, there are two coplanar designs for 4-bit RCA. The first design has been proposed in [33] that contains 209 cells with 1.25 clock cycle delay, while the second design has been proposed with 212 cells and 5 clock cycle delay [30]. In 2019, a multilayer QCA design for 4-bit RCA with 125 cells and with 5 clock cycle delay has been proposed [31]. The design in [31] is more efficient than the other previous designs in terms of cell count.

Many QCA designs have been proposed for 8-bit and 16-bit RCA in [25, 29, 30, 34, 35]. In 2012, a QCA multilayer design for 8-bit RCA with 695 cells and 3 clock cycle delay and a QCA for 16-bit RCA design consists of 1759 with 5 clock cycle delay [35]. In 2015, a QCA coplanar design for 8-bit RCA with 572 and 11 clock cycle delay and a QCA design for 16-bit RCA design contains 1336 cells with 19 clock cycle delay [25]. In 2016, a QCA multilayer design for 8-bit and 16-bit RCA have been proposed. The 8-bit QCA design consists of 517 with 10 clock cycle delay, while the 16-bit design consists of 1224 with 18 clock cycle delay [29]. In 2018, a QCA coplanar design for 8-bit and 16-bit RCA have been proposed in [30]. The 8-bit RCA contains 513 cells with 9 clock cycle delay and the 16-bit RCA consists of 1401 with 17 clock cycle delay.

In [12-35], there are many problems in the QCA designs such as multilayers mode used in the construction, many cells used in the design, number of majority gates, and the clock cycle delay. The aim of this paper is to propose QCA designs for XOR, half-adder, full adder, and RCA circuits with better cell count and clock cycle delay.

3 QCA Background

QCA circuit wires and the computational components are constructed using QCA cells. A QCA cell with four quantum dots and two mobile electrons positioned in the corners is the basic element of a QCA system. By applying an appropriate electric neighborhood field at the tunneling intersections, the potential boundaries control the movement of mobile electrons to supply the individual cell with three states. The primary state is invalid cell which occurs when the boundaries are decreased by reducing the electrical field, allowing electrons to be detected at any point. The second state is positive polarization (P=+1), when the boundaries are emphatically raised while the third state is negative polarization (P=-1) that occurs when the boundaries are raised in opposite directions.

The expressions positive polarization and negative polarization are independently compared to the binary logic values ‘1’ and ‘0’ respectively. Figure 1 displays the basic QCA cells and their possible polarizations. The Coulombic interaction between the cells placed close to each other to allow the cells to be constrained to coordinate polarizations [6].

Equation 1 shows the kick energy which is produced by the Coulombic interaction between QCA cells and is computed by electrostatic interaction between all the electrons in the two nearby cells *i* and *j* [36], as follows:

$$E^{i,j}=\frac{1}{4\pi\varepsilon 0\,\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_n{}^{i}q_m{}^{j}}{¿\,r_n{}^{i}-r_m{}^{j}\vee¿} \quad (1)$$

Where ε_0 is the permittivity of free space, ε_r is the dielectric constant, $q_n{}^{i}$ is the charge in dot n of cell i, $r_n{}^{i}$ is the position of dot n in cell i and $¿\,r_n{}^{i}-r_m{}^{j}\vee¿$ is the distance between cells. Equation 2 is the kink energy between two cells as the energy difference between two cells with different polarity or the same two cells with the same polarization [36].

$$Ekink^{i,j}=E^{i,j}{}_{Pi\neq Pj}-E^{i,j}{}_{Pi=Pj} \quad (2)$$

Where E is energy, P_i is the polarization of cell i, and P_j is the polarization of cell j. Equation 3 can be used to calculate the polarization of each cell [36].

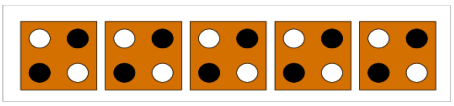
$$P_i=\frac{\frac{Ekink^{j,j}}{2\gamma}\sum jP_j}{\sqrt{1+¿¿¿}} \quad (3)$$

Where P_i is the polarization state of the cell, P_j is the polarization state of the neighboring cell, and γ is the tunneling energy of electrons within the cell.

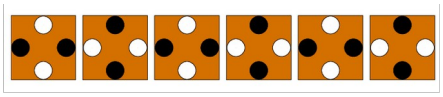
Figure 1: QCA cell polarization.

Due to the Coulombic interactions between cells in a QCA wire, binary information is transfered from input to output. Figure 2a demonstrates the propagation with a 90 ° QCA wire. A 45° QCA wire is also possible where the binary signal transmission alternates between the two separate polarizations +1 and -1 as shown in Figure 2b. The intersection of two wires in a single layer is shown in Figure 3a, while the two wires that are not contacting with each other is called multilayer mode where the data is sent through the “via” layer, which serves as a bridge as shown in Figure 3b [36]. A QCA circuit is designed by arranging QCA cells in a Cartesian plane. The entire array can relax to their ground state once the QCA input cells are in fixed polarization and data can be read by measuring the output cell. The primary difference between the input and output cells is that the input cells have fixed polarization, whereas the output cells can be switched to any polarization that returns the system to its ground state [6]. A common QCA gate known as a 3-input majority function is the QCA majority (QM) gate. As shown in

Figure 4a, this gate consists of five QCA cells with a cross-shaped structure. The five cells are divided into three input cells, one output cell, and one device cell. Suppose that the three inputs are *a*, *b*, and *c*, at that point the logic function of the QM gate is $M(a, b, c) = a.b+b.c+a.c$, where $a+b$ indicates *a* OR *b*, and $a.b$ indicates *a* AND *b* [37]. The polarity of the device cell is determined by the Coulombic repulsion which are equivalent to the polarities of the majority of three input cells. The polarity of device cell is moved toward the output cell. Building the OR and the AND gates by setting the polarization of one of the QM gate inputs to $P=+1$ (logic "1") and $P= -1$ (logic "0"), as shown in Figure 4b and Figure 4c respectively. Another QCA gate is the NOT gate or the inverter as shown in Figure 5. The NAND gate can be developed utilizing the AND gate followed by the NOT gate as shown in Figure 6 [38].

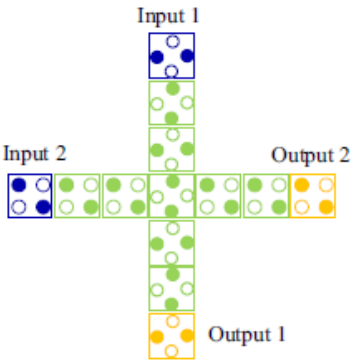


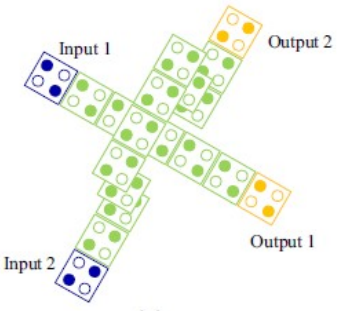
(a)



(b)

Figure 2: QCA wire (a) wire (90°), (b) wire (45°).





(a) (b)

Figure 3: Intersection wire (a) single layer, (b) multilayer

(a) (b) (c)

Figure 4: Using QM gate to construct logic gates: (a) QM gate, (b) OR gate, and (c) AND gate.

Figure 5: QCA inverters.

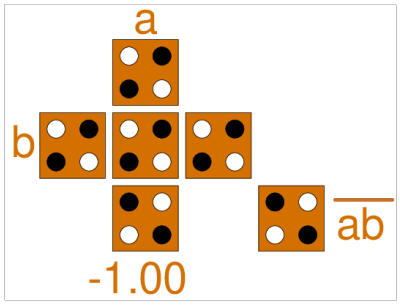


Figure 6: QCA layout of NAND gate.

The clocking of QCA can be achieved by measuring the capacity barriers to the connected quantum-dots. Increasing or decreasing the potential obstruction allows full localization control for the polarization of the free electrons. A QCA cell has 4 stages of clocking named Switch, Hold, Release, and Relax. During the Switch stage, the dots barrier is gradually formed to put the electrons to the corners so that the cell is at final polarization of the adjacent cell. In the Hold stage, the cell is still in polarization and affects the adjacent cells during the increase of the barriers. The Release stage causes the electrons to move to the middle dots because the barriers are decreased causing the cells to lose polarization. The fourth stage is the Relax stage where the electrons move to the middle dots making the cell to be in no definite polarization [37]. Figure 7 represents a cell in its four clock phases.

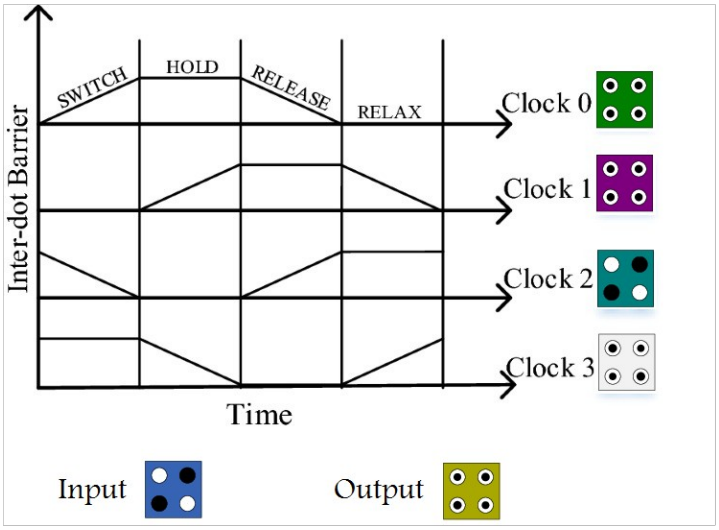


Figure 7: The four phases of the

4 Proposed QCA for Arithmetic Circuits

Arithmetic addition is the most important arithmetic operation in computation. In this section, QCA designs for XOR gate, half adder circuit, full adder circuit, and RCA with different sizes circuits will be shown. In this paper, QCADesigner tool version 2.0.3 is used to outline and simulate the proposed QCA designs circuits running the framework with coherence simulation engine [39]. The entire simulation computations and parameters have been set to their default values in the QCADesigner-E simulator. The defined parameters in Table 1 were used for "Coherence Vector" because for every time step the relaxation time and steady state of each cell are calculated and the coherence vector for each cell is stepped forward in time [40, 41].

Table 1: Parameters used in simulation of proposed QCA circuits.

Temperature (K)	1.000000
Cell Width (nm)	18.000000
Cell Height (nm)	18.000000
Relaxation Time (S)	1.000000×10^{-15}
Time Step (S)	1.000000×10^{-16}
Total Simulation Time (S)	7.000000×10^{-11}
Clock High (J)	9.800000×10^{-22}
Clock Low (J)	3.800000×10^{-23}
Clock Shift	0.000000
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000

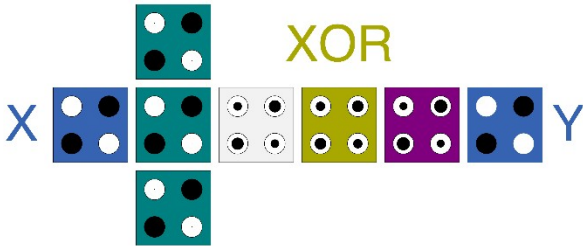
(nm)	
Relative Permittivity	12.900000
Layer Separation (nm)	11.500000

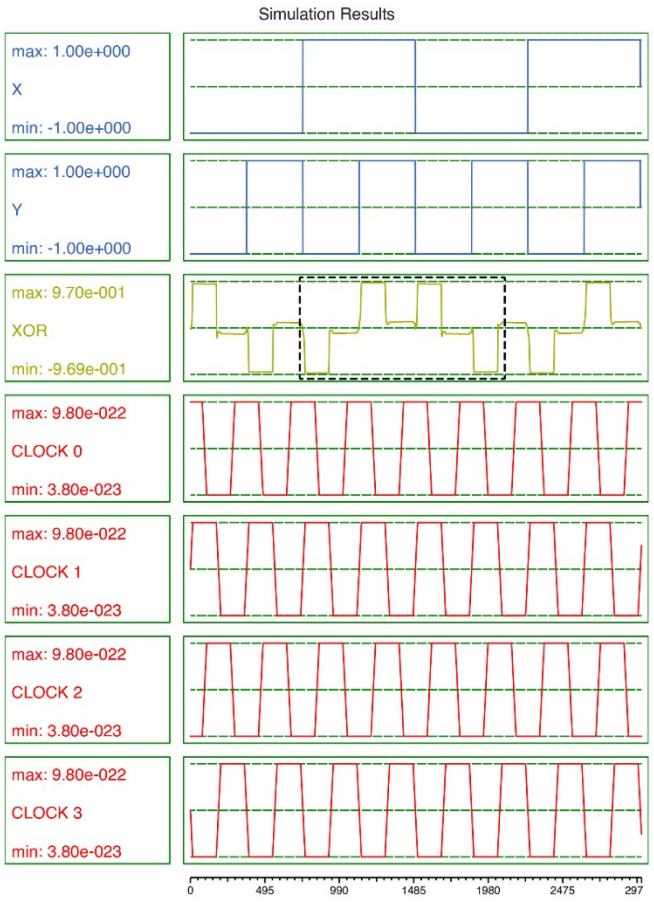
4.1 XOR Gate

The exclusive disjunction gate, also known as the XOR gate, is a logical function with two inputs that returns a logical value of true if and only if one of the inputs has a value of true, or returns a logical value of false if both inputs are true or both inputs are false, and is symbolized by $\oplus$. The truth table of the XOR gate is shown in Table 2. Figure 8a presents the proposed QCA design of XOR gate that consists of 8 cells and with 2 clock cycle delay while Figure 8b presents the simulation results. Correct QCA layout is dependent on the proper clocking zone. As a result, the timing rules play a significant role in QCA design guidelines [42]. The cells of the proposed design with different clock cycle work together to generate the correct output of XOR gate without using QM gate. Comparing the proposed design with related QCA designs is shown in Table 3. The following sections show the design of QCA adder circuits based on the proposed QCA for the XOR gate.

Table 2: Truth table of XOR gate.

X	Y	X $\oplus$ Y
0	0	0
0	1	1
1	0	1
1	1	0





(a) (b)

Figure 8: XOR gate: (a) The proposed QCA design, (b) the simulation results.

Table 3: Comparison between the proposed QCA design for the XOR gate with other designs.

QCA design for XOR gate	Complexity (Cell count)	Cell area (nm^2)	Latency (Clocking Cycles)	No. of QM gate	Wire crossover
Figure 13 in [12]	32	10,368	1	1	Not Required
Figure 7b in [13]	28	9,072	0.75	2	Not Required
Figure 2b in [14]	12	3,888	0.5	0	Coplanar
Figure 3a in [15]	17	5,508	2	1	Coplanar
Figure 2 in [16]	9	2,916	0.25	0	Coplanar
Figure 11 in [17]	26	8,424	3	3	Coplanar
The proposed design in Figure 8	8	2,592	2	0	Coplanar

4.2 Half Adder Circuit

The half adder circuit depends on the XOR gate which is the basic component in arithmetic addition operation. The half adder circuit has two input variables X and Y, and two output variables SUM and $CARRY$. Equation 4 shows the logic operation of half adder circuit and its truth table is shown in Table 4. The proposed QCA design for half adder circuit consists of 20 cells with 2 clock cycle delay as shown in Figure 9a and the simulation results is shown in Figure 9b. To produce the desired output for $CARRY$, the proposed QCA design for half adder circuit contains one QM gate that acts as an AND gate between the two inputs X and Y.

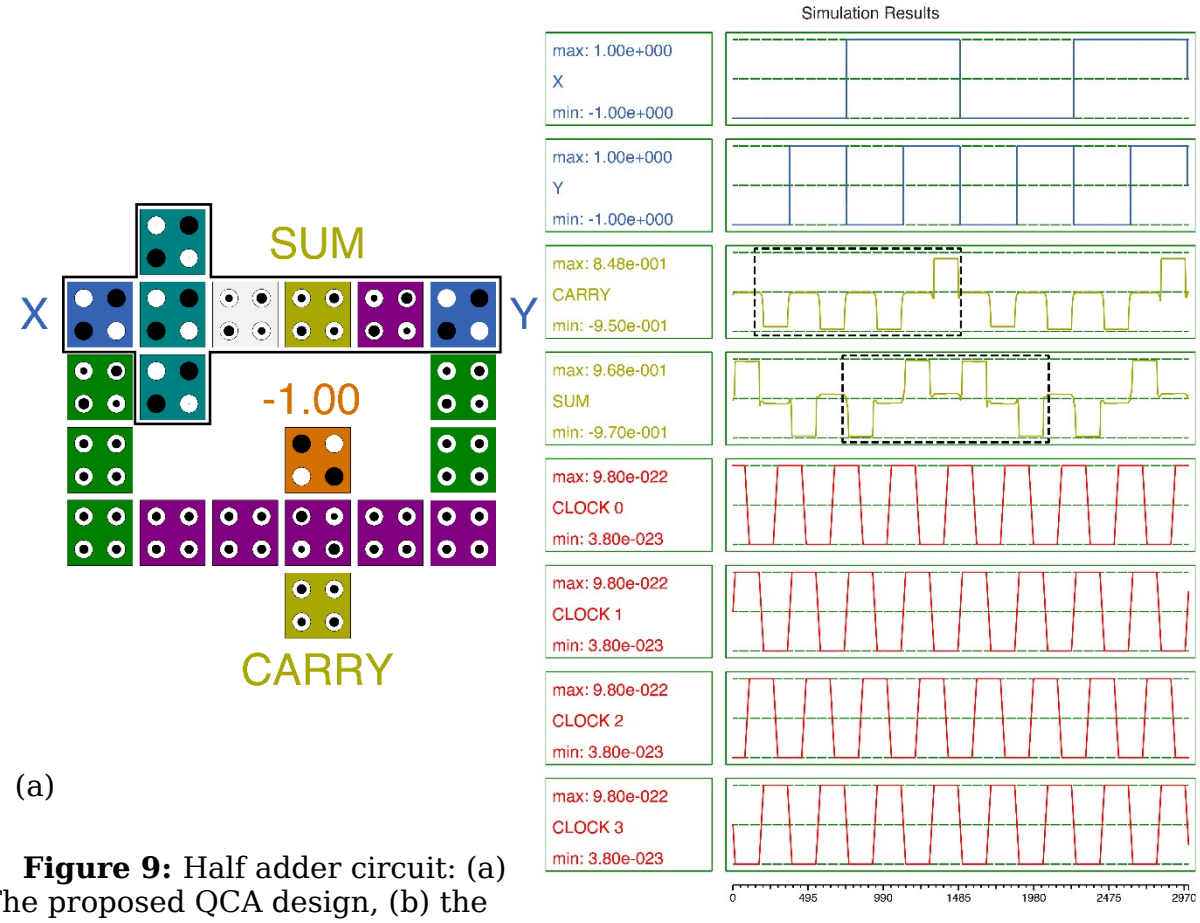
Table 5 compares the proposed design for the half adder circuit with related QCA designs.

$$SUM = X \oplus Y \quad (4)$$

$$CARRY = X.Y$$

Table 4: Truth table of half adder circuit.

X	Y	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



(a)

Figure 9: Half adder circuit: (a) The proposed QCA design, (b) the simulation results.

Table 5: Comparison between the proposed QCA design for the half adder circuit with other designs.

QCA design for half adder circuit	Complexity (Cell count)	Cell area (nm^2)	Latency (Clocking Cycles)	No. of QM gate	Wire crossover
Figure 10 in [18]	77	24,948	4	2	Multilayer
Figure 5a in [19]	62	20,088	2	1	Coplanar
Figure 8a in [20]	40	12,960	1	4	Coplanar
Figure 17 in [21]	27	8,748	0.5	2	Coplanar
Figure 8 in [22]	48	15,552	0.5	3	Coplanar
Figure 4 in [23]	26	8,424	0.5	2	Coplanar
The proposed design in Figure 9	20	6,480	2	1	Coplanar

4.3 Full Adder Circuit

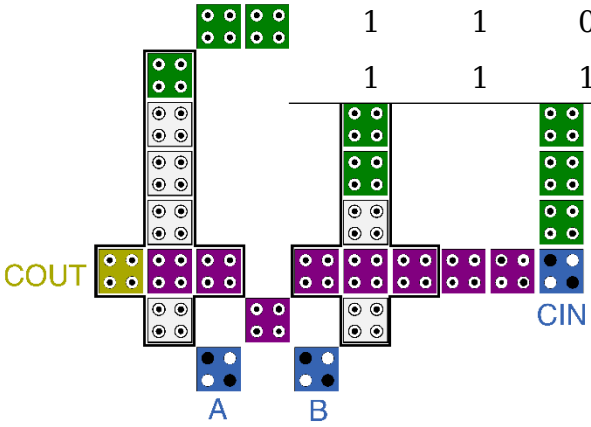
The full adder circuit has three input variables *A*, *B*, and *CIN*, and two output variables *SUM* and *COUT*. Equation 5 shows the logic operation of the full adder circuit and its truth table is shown in Table 6. The proposed QCA design for full adder circuit is based on the QCA design of the proposed XOR gate. The proposed QCA design for full adder circuit consists of two XOR gates to generate the correct output.

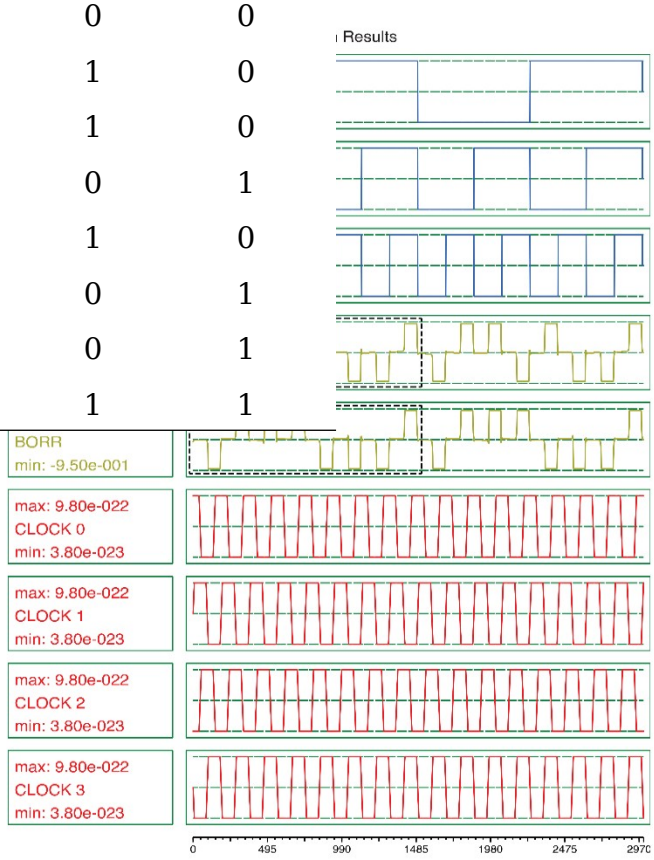
$$SUM=A \oplus B \oplus CIN \quad (5)$$
$$COUT=A.B+A.CIN+B.CIN$$

The proposed QCA design for full adder consists of 36 cells with 0 clock cycle delays and single QM gate as shown in Figure 10a and the simulation results are shown in Figure 10b. The QM gate is used in the construction to get the output *COUT*. Table 7 compares the proposed design with related QCA designs for the full adder circuit**.**

Table 6: Truth table of full adder circuit

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1





(a) (b)

Figure 10: Full adder circuit: (a) The proposed QCA design, (b) the simulation results.

Table 7: Comparison between the proposed QCA design for the full adder circuit with other designs.

QCA design for full adder circuit	Complexity (Cell count)	Cell area (nm^2)	Latency (Clocking Cycles)	No. of QM gate	Wire crossover
Figure 12 in [18]	122	39,528	4	2	Multilayer
Figure 6b in [24]	69	22,356	1	3	Coplanar
Figure 8a in [25]	59	19,116	1	3	Coplanar
Figure 2 in [26]	63	20,412	0.25	2	Coplanar
Figure 9 in [29]	38	12,312	3	3	Multilayer
Figure 5 in [28]	33	10,692	0.5	3	Coplanar
Figure 9 in [27]	47	15,228	1.5	7	Multilayer
Figure 3c in [30]	40	12,960	2	3	Coplanar
Figure 13 in [31]	25	8,100	2	1	Multilayer
Figure 4b in [15]	49	15,876	4	1	Coplanar
Figure 15a in [32]	30	9,720	0.5	3	Multilayer
Figure 13 in [17]	86	27,864	3	4	Coplanar
The proposed design in Figure 10	36	11,664	0	1	Coplanar Multilayer

4.4 Ripple Carry Adder (RCA) Design

Ripple carry adders of various sizes can be easily created using a QCA full-adder. Figure 11 shows that four QCA full-adders are used to create the QCA design of 4-bit ripple carry adders with 182 cells. *CIN*, *A0- A3*, and *B0-B3* are the inputs in this design. The output values of the proposed design are *S0-S3* and *COUT*. The *CIN* input value of a QCA full-adder is the *COUT* output value of the previous QCA full-adder. The proposed QCA 4-bit RCA design has 4 QM gates and 1 clock cycle delays to produce the desired output as shown in Figure 12. Table 8 compares the proposed design with related QCA designs for the 4-bit RCA.

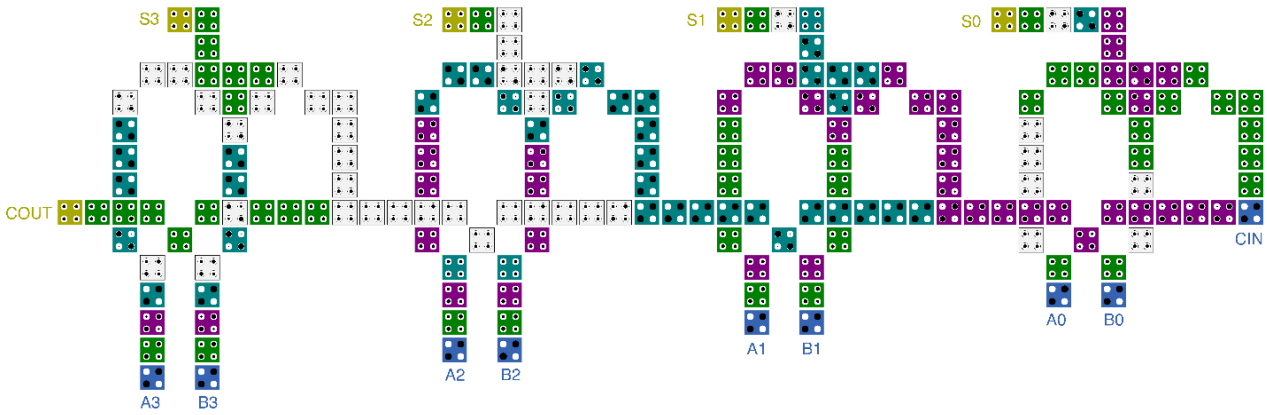


Figure 11: The QCA design of a 4-bit RCA using the proposed QCA full-adder in Figure 10.

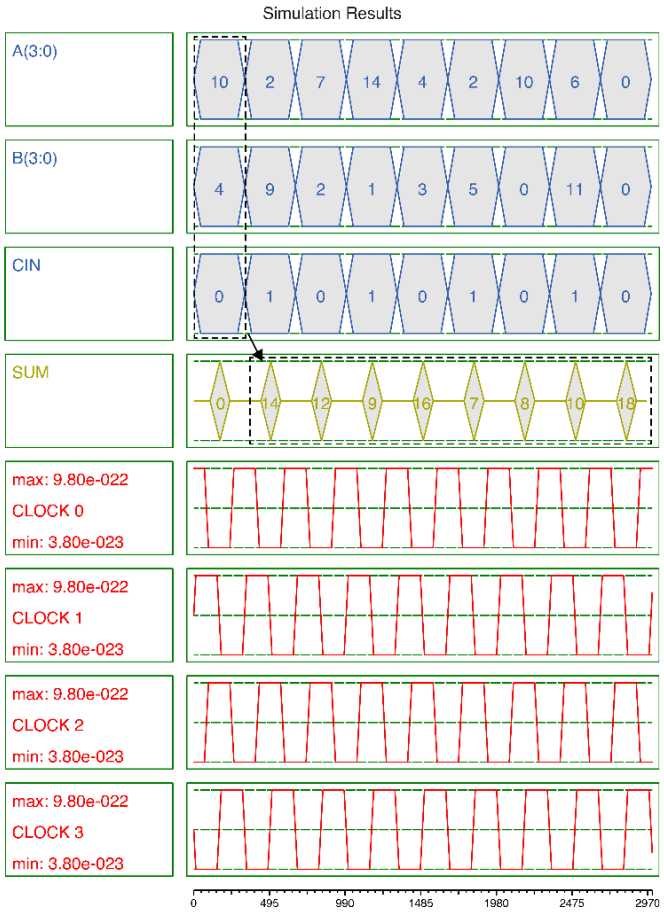


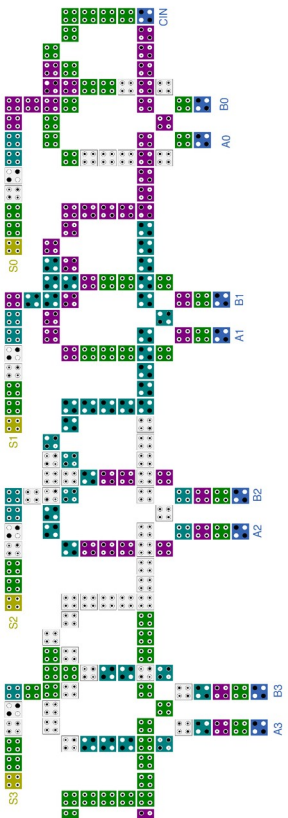
Figure 12: The Simulation results of the proposed 4 bit RCA presented in Figure 11.

Table 8: Comparison between the proposed QCA design for RCA 4 bit with other designs.

QCA design for RCA 4 bit	Complexity (Cell count)	Cell area (nm^2)	Latency (Clocking Cycles)	No. of QM gate	Wire crossover
Figure 13 in [29]	237	76,788	6	12	Multilayer
Figure 6 in [28]	175	56,700	5	12	Multilayer
Figure 5b in [30]	212	68,688	5	12	Coplanar
Figure 13 in [33]	209	67,718	5	4	Coplanar
Figure 14 in [31]	125	40,500	1	4	Multilayer
The proposed design in Figure 11	182	58,968	1	4	Coplanar

Larger QCA ripple carry adders can be constructed. In the following, QCA designs for 8-bit and 16-bit ripple carry adders have been proposed. Figure 13 shows the QCA layout of an 8-bit RCA, with the inputs denoted by CIN, A0- A7, and B0-B7. The output values of the proposed design are S0-S7 and COUT. This design consists of 449 cells with 2 clock cycle delay.

Figure 14 shows the QCA layout of a 16-bit RCA, with the inputs denoted by CIN, A0-A15, and B0-B15. The output values of the proposed design are S0-S15 and COUT. This design has 1269 cells and requires 4 clock cycle delay to produce the desired output. Table 9 compares the proposed design of the ripple carry adders for 8-bit and 16-bit sizes with related QCA designs.


CIN
B0
A0
S0
B1
A1
S1
B2
A2
S2
B3
A3
S3

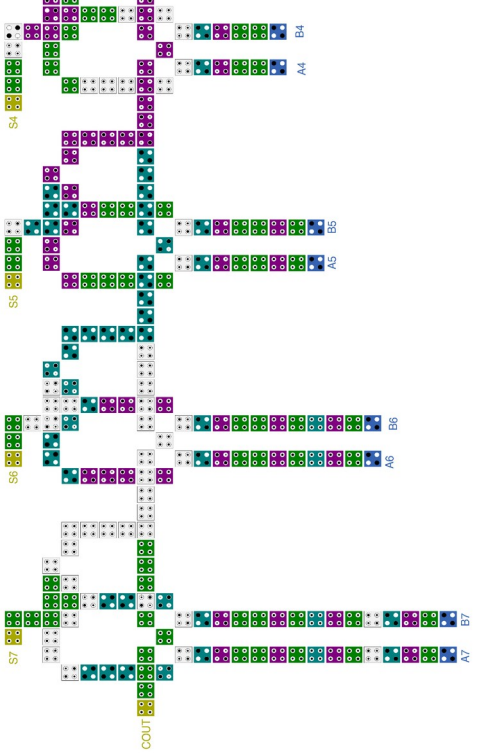


Figure 13: The QCA design of an 8-bit RCA using the proposed QCA full-adder in Figure 10.

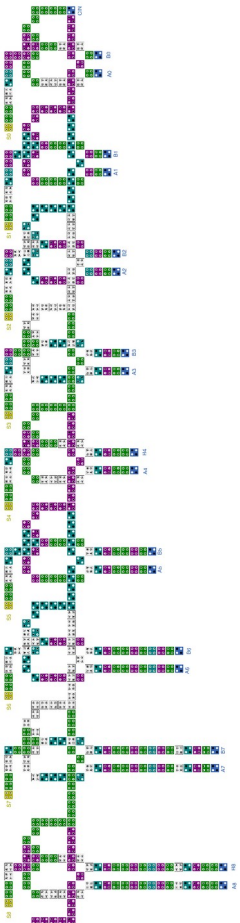


Figure 14: The QCA design of a 16-bit RCA using the proposed QCA full-adder in Figure 10.

Table 9: Comparison between the proposed QCA design for RCA 8 bit and 16 bit with other designs.

QCA design for RCA		Complexity (Cell count)	Cell area (nm^2)	Latency (Clocking Cycles)	Wire crossover
RCA 8 bit	In [35]	695	225,180	3	Multilayer
	In [34]	1606	520,344	8	Multilayer
	In [25]	572	185,328	11	Coplanar
	In [29]	517	167,508	10	Multilayer
	In [30]	513	166,212	9	Coplanar
	The proposed design in Figure 13	449	145,476	2	Coplanar
RCA 16 bit	In [35]	1759	569,916	5	Multilayer
	In [34]	3587	1,162,188	12	Multilayer
	In [25]	1336	432,864	19	Coplanar
	In [29]	1224	396,576	18	Multilayer
	In [30]	1401	453,924	17	Coplanar
	The proposed design in Figure 14	1269	411,156	4	Coplanar

5 Energy Dissipation Analysis

The energy dissipation is calculated using the QCADesigner-E tool simulator [43]. This application is based on earlier studies by Timer and Lent which is intended to estimate the power dissipation of QCA circuits [41, 44]. In this paper, QCADesigner-E tool is used to calculate the total energy dissipation, average energy dissipation per cycle, total simulation time, total error, and average error for all the proposed circuits as shown in Table 10.

Table 10: Energy dissipation of all the proposed desgins.

Energy Dissipation	Total (eV)	Average per cycle (eV)	Total simulation time per second	Total error (+/-) eV	Average error (+/-) eV
XOR gate	4.45×10^{-3}	4.05×10^{-4}	13	-3.96×10^{-4}	-3.60×10^{-5}
Half adder circuit	1.96×10^{-2}	1.79×10^{-3}	33	-2.04×10^{-3}	-1.85×10^{-4}
Full adder circuit	2.83×10^{-2}	2.58×10^{-3}	60	-2.92×10^{-3}	-2.65×10^{-4}
4-bit RCA	7.38×10^{-2}	6.71×10^{-3}	310	$-6.96 \times$	$-6.33 \times$
8-bit RCA	$20.35 \times$	17.44×10^{-3}	630 1575		

16-bit RCA	10^{-2}	45.35× 10^{-3}	10^{-3}	10^{-4}
	52.93× 10^{-2}		-16.01 × 10^{-3}	-14.55× 10^{-4}
			-36.82× 10^{-3}	-33.46× 10^{-4}

6 Conclusion

In this paper, a QCA design for XOR gate, half adder, full adder, and various sizes of RCA circuits such as 4 bit, 8 bit, and 16 bit have been proposed. The proposed QCA XOR gate has been used to implement a QCA half adder circuit and a QCA full adder circuit. The QCA half adder is used to make the computation of addition between two inputs while the QCA full adder is used to make the computation between three inputs. A QCA RCA circuits of sizes 4-bit, 8-bit, and 16-bit have been proposed using the proposed QCA full adder. Other related designs are compared with the proposed designs. The comparisons showed that the proposed QCA designs are better in terms of number of cells utilized, wire crossing mode, number of QM gates, area used by QCA cells, and/or the clock cycle delay. More errors about the interaction of QCA design occur due to the presence of minor faults. The correct approach to reduce such errors is to create QCA design that gives the correct output in the presence of errors by replacing all cells that are faults with others cells that are in correct state. As future work for this paper is to use an improved version of all the proposed QCA designs to generate the right output summation in the presence of faults.

Conflicts of Interest: The authors declare no competing financial interest. The authors declare that they have no conflict of interest.

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